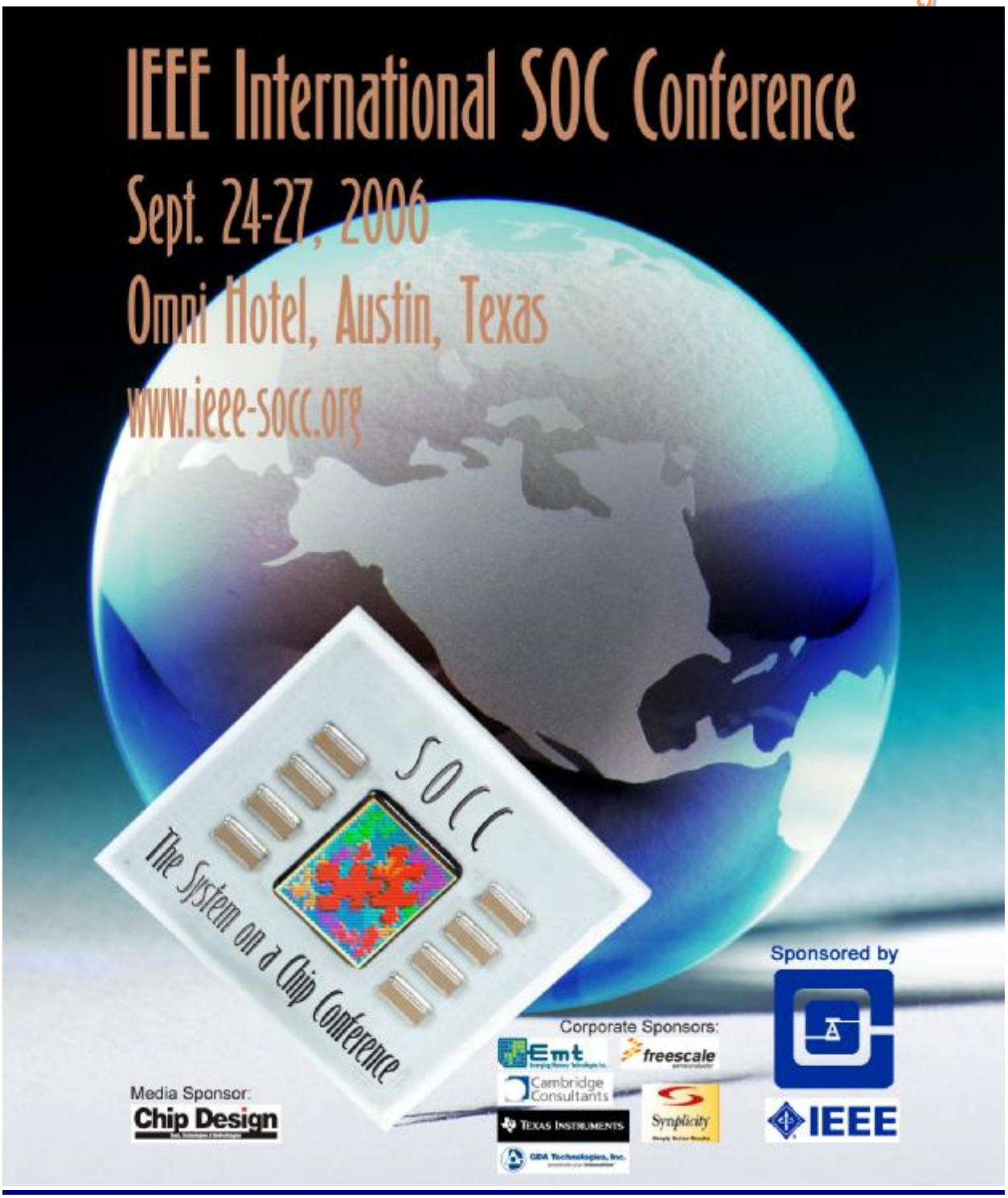
IEEE SOCC 2006

Advance Program



SUNDAY, SEPTEMBER 24
Workshop Tutorials

Tutorial Track A

8:00 – 10:00
SA1: **RAM-based Circuits and Architectures for Multimedia and Signal Processing SOCs,** *Martin Margala, University of Rochester*

10:30 – 12:30PM
SA2: **High-performance energy-efficient memory circuit technologies for sub-45nm technologies,** *Amit Agarwal and Ram Krishnamurthy, Intel Corporation*

2:00 – 5:00PM
SA3: **Chip-level and Input/Output Interconnects for Gigascale SOCs:Limits and Opportunities,** *Azad Naeemi and Muhannad Bakir, Georgia Institute of Technology*

Tutorial Track B

8:00 – 10:00
SB1: **Design of Digital PLLs for Low Power Applications**, *Krishnasawamy Nagaraj, Texas Instruments Inc.*

10:30 – 12:30PM
SB2: **Silicon Debug and DFT Tutorial for SOC IP Providers,** *Nikhil Dakwala, Stridge*

2:00 – 5:00PM
SB3: **On-chip Distributed Communication-Architectures, Services and Design Methodologies,** *Tiberiu Seceleanu, University of Turku (UTU), Finland*

MONDAY, SEPTEMBER 25

PLENARY SESSION
8:15 a.m. - 11:30 a.m.

08:15 **Opening Remarks**: Ram Krishnamurthy, General Conference Chair
Technical Program Overview: Suhwan Kim, Technical Program Chair

08:30 **Keynote Presentation**: "**How the Shrinking System is Creating an Expanding Market"**

Gene Frantz
Principal Fellow, Texas Instruments, Inc.

09:30 **Plenary Presentation: "Curing the ailments of nanometer CMOS through self-healing and resiliency"**

Professor Jan Rabaey
Professor and Director of GigaScale Systems Research Center (GSRC), University of California at Berkeley

10:30 **Plenary Presentation:** *(title to be announced)*

Jim Kahle
IBM Fellow and Director of Technology, STI Design Center for Cell Technology, IBM Corporation

MONDAY, SEPTEMBER 25

CONCURRENT SESSIONS
01:00 p.m. – 2:40 p.m.

SESSION MA2: Analog Design For SOC

Chair: *Hongjiang Song, Intel Corporation*
Co-chair: *Ramalingam Sridhar, SUNY at Buffalo*

1:00P **A 120nm CMOS Fully Differential Rail-to-Rail I/O Opamp with Highly Constant Signal Behavior**
MA2.1 *Weixun Yan, Horst Zimmermann, Vienna University of Technology*

1:25P **A CMOS Low-Noise, Low-Dropout Regulator for Transceiver SOC Supply Management**
MA2.2 *Wonseok Oh, Bertan Bakkaloglu, Bhaskar Aravind*, Siew Kuok Hoon*, Arizona State University, *Texas Instruments Inc.*

SESSION MB2: DSP and Embedded Systems

Chair: *Ken Hsu, Rochester Institute of Technology*
Co-chair*: Thanh Tran, Texas Instruments Inc*

1:00P **Energy-Aware MPEG-4 Single Profile In HW_SW Multi-Platform Implementation**
MB2.1 *Antoni Portero, Guillermo Talavera, Marius Montón, Borja Martínez, Marc Moreno, Francky Cathoor*, Jordi Carrabina, Universitat Autónoma of Barcelona, *IMEC vzw, Leuven*

1:25P **A Real Time Programmable Encoder for Low Density Parity Check Code as specified in the IEEE P802.16E/D7 Standard and its Efficient Implementation on a DSP Processor**
MB2.2 *Zahid Khan, Tughrul Arslan, *Scott MacDougall, University of Edinburgh, and *Freescale Semiconductor UK Limited EastKilbride*

1:50P **Efficient FPGA-Based Realization of Complex Squarer and Complex Conjugate Using Embedded Multipliers**
MB2.3 *Shuli Gao, Dhamin Al-Khalili, Noureddine Chabini, and Pierre Langlois*, Royal Military College of Canada, *École Polytechnique de Montréal*

2:15P **Architecture for Low Power Large Vocabulary Speech Recognition**
MB2.4 *Dhruba Chandra, Ullas Pazhayaveetil, Paul D. Franzon, North Carolina State University*

2:40-3:00P COFFEE BREAK

MONDAY, SEPTEMBER 25

CONCURRENT SESSIONS
03:00 p.m. – 4:45 p.m.

SESSION MA3: RF Circuits and Systems

Chair: *Tobias G. Noll, RWTH Aachen University, Germany*
Co-chair: *Sakir Sezer, Queen's University Belfast*

3:00P **A General Method to VLSI Polyphase Filter Analysis and Design for Integrated RF Applications**
MA3.1 *Hongjiang Song, Intel Coporation*

3:25P **I/Q-Channel Mismatch Transfer and Amplification Effects and Applications to the Measurement and Calibration of Integrated VLIF RF Receivers**
MA3.2 *Hongjiang Song, Syed Roomi Naqvi, Bertan Bakkaloglu*, Intel Coporation, *Arizona State University*

3:50P **A Dual-Function Filter For 5.25GHZ Narrowband and 3.6GHZ-10.1GHZ Ultrawideband Systems**
MA3.3 *Anh Dinh, Bi Pham, University of Saskatchewan, Saskatchewan, Canada*

4:15P **Architecture and Implementation of Power and Area Efficient Receiver Equalization Circuit for High-Speed Serial Data Communication**
MA3.4 *Hongjiang Song, Intel Coporation*

SESSION MB3: Network and Reconfigurable Architectures

Chair: *Tughrul Arslan, University of Edinburgh, Scotland, UK*

Co-chair: *Koushik K. Das, IBM Corporation*

3:00P **H.264 Decoder Implementation on a Reconfigurable Instruction Cell Architecture**
MB3.2 *Adam Major, Ying Yi, Ioannis Nousias, Mark Milward, Sami Khawam and Tughrul Arslan, University of Edinburgh*

3:25P **A Compact and High-Performance Switch for Circuit-Switched Network On Chip**
MB3.3 *Phi-Hung Pham, Yogendera Kumar and Chulwoo Kim, Korea University*

3:50P **Cell Switched Network-On-Chip – Candidate For Billion-Transistor System-On-Chips**
MB3.4 *Yuhua Chen, University of Houston*

POSTER SESSION AND CONFERENCE RECEPTION

4:45 - 6:00P
Chair: *Ram Krishnamurthy, Intel Corporation*
Co-chair: *Thanh Tran, Texas Instruments*

P.1 **An On-Chip Measurement Circuit for Calibration by Combination Selection**, *Janne Maunu*+, Joona Marku*+, Mika Laiho*, Ari Paasio*, *University of Turku, +Turku Centre for Computer Science, TUCS*

P.2 **A Novel Mini-LVDS Receiver in 0.35-um CMOS**, *Chung-Yuan Chen, Jia-Hong, Tai-Ping Sun, National Chi Nan University, Taiwan*

P.3 **A Reconfigurable CMOS Power Amplifier Operating From 0.9 to 2.4 GHZ For WPAN Application**, *Seok-Oh Yun and Hyung-Joun Yoo, Information and Communications University, Korea*

P.4 **A Pulse-Based Full-Band UWB Transceiver SOC in 0.18um SiGe BiCMOS**, *Haolu Xie, Siqiang Fan, Xin Wang, Albert Wang, Zhihua Wang* and Hongyi Chen*, Illinois Institute of Technology, *Tsinghua University*

P.5 **Energy-Aware Code Replication for Improving Reliability in Embedded Chip Multiprocessors**, *Guilin Chen, Ozcan Ozturk, Guangyu Chen, Mahmut Kandemir, Pennsylvania State University*

P.6 **Optimal Multiple-Bit Huffman Decoding,** *Ya-Nan Wen, Sao-Jie Chen, Yu-Hen Hu*, National Taiwan University, *University of Wisconsin Madison*

P.7 **A Leakage Compensation Technique for Dynamic Latches and Flip-flops in Nano-scale CMOS**, *Martin Hansson and Atila Alvandpour, Linköping University*

P.8 **Stochastic Glitch Estimation and Path Balancing for Statistical Optimization**, *Hosun Shin, Naeun Zang*,, Juho Kim*, , Samsung Electronics, *Sogang University.*

P.9 **Supply and Threshold Voltage Optimization for Temperature Variation Insensitive Circuit Performance: A Comparison**, *Ranjith Kumar and Volkan Kursun, University of Wisconsin at Madison*

P.10 **Analysis Of Subthreshold Finfet Circuits For Ultra-Low Power Design**, *Xiaoxia Wu, Feng Wang, Yuan Xie, Pennsylvania State University*

P.11 **Design of Ultra-Low Power Combinational Standard Library Cells Using A Novel Leakage Reduction Methodology**, *Preetham Lakshmikanthan, Karan Sahni and Adrian Nuñez, VSDCAD Laboratory, EECS Department, Syracuse University*

P.12 **Method For Managing Electromigration in SOC's When Designing for both Reliability and Manufacturing**, *Karen Chow, David Abercrombie, Mark Basel, Mentor Graphics Corporation*

P.13 **Automatic Synthesis of Interface Circuits From Simplified IP Interface Protocols and Matching Information**, *ChangRyul Yun, YoungHwan Bae*, HanJin Cho*, and KyoungSon Jhang, ChungNam National University, *Multimedia SOC Design Team, ETRI*

P.14 **Performance Improvements Through Timing Driven Reconfiguration of Black-Boxes in Platform FPGAs**, *Priya Sundararajan, Sridhar Krishnamurthy*, N Vijaykrishnan,, Kamal Chaudhary* and Rajeev Jayaraman*, Pennsylvania State University, *Xilinx Inc.*

P.15 **A Reconfigurable Viterbi Trackback For Implementation On Turbo Decoding Array**, *Imran Ahmed, Tughrul Arslan*, University of Edinburgh, *Institute for System Level Integration*

P.16 **SoC Design Space Exploration Through Automated IP Selection from SystemC IP Library**, *Deepa. Mathaikutty and Sandeep Shukla, Virginia Tech University*

P.17 **A Design Methodology for a Low-Power, Temperature-Aware SoC Developed for Medical Image Processors**, *Zhenyu Qi, Wei Huang, Adam Cabe, Wenqian Wu, Yan Zhang, Garret Rose, Mircea R. Stan, University of Virginia*

P.18 **Geometric Tiling for Reducing Power Consumption in Structured Matrix Operations**, *G' Chen, L. Xue, J. Kim, K. Sobti*, L. Deng*, X. Sun**, N. Pitsianis**, C. Chakrabarti*, M. Kandemir, N. Vijaykrishnan, Pennsylvania State University, *Arizona State University, **Duke University*

P.19 **High Read Stability and Low Leakage SRAM Cell Based on Data/Bitline Decoupling**, *Zhiyu Liu and Volkan Kursun, University of Wisconsin at Madison*

TUESDAY, SEPTEMBER 26

CONCURRENT SESSIONS
08:30 a.m. – 10:10 a.m.

SESSION TA1: Mixed Signal Circuits and Systems

Chair: *Hongjiang Song, Intel Corporation*
Co-chair: *Yong-Bin Kim, Northeastern University*

8:30A **A Novel 8-Phase PLL Design for PWM Scheme in High Speed I/O Circuits**
TA1.1 *Rui Tang and Yong-Bin Kim, Northeastern University*

8:55A **A Timing Jitter Reduction Technique in a Cyclic Injection Clock Multiplier for Data Communication System**
TA1.2 *Qingjin Du, Jingcheng Zhuang, Tad Kwasniewski, Carleton University*

9:20A **Reconfigurable Switched-Capacitor ΔΣ Modulator Topology Design**
TA1.3 *Ying Wei, Pengbo Sun, Alex Doboli, Stony Brook University*

9:45A **A 1.3 V 30-mW 8-Bit 166-MS/s A/D Converter in 0.18 µm CMOS with Reference Generator**
TA1.4 *Li Jing-hu, Yu Ming-Yan, Wang Yong-Sheng, Wang Jin-Xiang, Harbin Institute of Technology*

SESSION TB1: Industrial SoC Applications and Methods

Chair: *Thomas Büchner, IBM*
Co-chair: *Radu M. Secareanu, Freescale*

8:30A Invited Paper: **"Multi-Project System-on-Chip (MP-SoC): A Novel Test Vehicle for SoC Silicon Prototyping"**
TB1.1 *Chun-Ming Huang, Kuen-Jong Lee*, Chih-Chyau Yang, Wen-Hsiang Hu, Shi-Shen Wang, Jeng-Bin Chen, Chi-Shi Chen, Lan-Da Van**, Chien-Ming Wu, Wei-Chang Tsai and Jing-Yang Jou, National Applied Research Laboratories, *National Cheng Kung University, **National Chiao Tung University*

8:55A **VLSI Architecture for Encryption and Watermarking Unit Towards the Making of a Secure Digital Camera**
TB1.2 *O. B. Adamo, S. P. Mohanty, E. Kougianos, and M. Varanasi, University of North Texas*

9:20A **A Trace-Driven Validation Methodology for Multi-Processor SoCs**
TB1.3 *Jayanta Bhadra, Ekaterina Trofimova, Leonard J. Giordano and Magdy S. Abadir, Freescale Semiconductor Inc.*

9:45A **Embedded Controllers for Solving Complex Industry Applications,**
TB1.4 *J. Saalmueller, J. Wuertz, IBM Development Lab*

10:10-10:30A COFFEE BREAK

TUESDAY, SEPTEMBER 26

CONCURRENT SESSIONS
10:30 a.m. – 11:45 a.m.

SESSION TA2: Low Power Design Techniques

Chair: *Xun Liu, North Carolina State University*

Co-chair: *Martin Margala, University of Rochester*

10:30A Invited Paper: **"Low-Power and Process Variation Tolerant Memories in sub-90nm Technologies"**
TA2.1 *Saibal Mukhopadhyay, Swaroop Ghosh, Keejong Kim, and Kaushik Roy, Purdue University*

10:55A **A Low Complexity, Low Power, Programmable QRS Detector Based on Wavelet Transform for Implantable Pacemaker IC**
TA2.2 *H. T. Tung, J. P. Son, Y. R. Kang, C. R. Kim, H. Y. Chung H.Y, S. W. Kim, Korea University, Korea*

11:20A **Leakage Reduction for Domino Circuits in sub-65nm Technologies**
TA2.3 *Manjari Agarwal, Praveen Elakkumanan and Ramjalingam Sridhar, University at Buffalo (SUNY)*

SESSION TB2: System Level Design Methodology

Chair: *Sao-Jie Chen,* National Taiwan University

Co-chair: *Kaijian Shi, Synopsys, Inc*

10:30A Invited Paper: **"Applying ESL in A Dual-Core SoC Platform Designing"**
TB2.1 *Alan P. Su, Robert Chen*, Springsoft Inc.*SoC Technology Center, ITRI*

10:55A **Bit-Width Aware High-Level Synthesis for Digital Signal Processing Systems**
TB2.2 *Bertrand Le Gal , Caaliph Andriamisaina*, Emmanuel Casseau*, Rennes I University France, *UBS University, France*

11:20A **Process Variation Aware Parallelization Strategies for MPSoCs**
TB2.3 *Suresh Srinivasan, Raghavan Ramadoss and N. Vijaykrishnan, Pennsylvania State University*

11:45-1:15P **CONFERENCE LUNCHEON**

Luncheon Presentation: **The Wild West Days of *NASA***
By: Dr. H. Dean Cubley, Chairman of Eagle RF Inc

TUESDAY, SEPTEMBER 26

CONCURRENT SESSIONS
1:30 p.m. – 3:10 p.m.

SESSION TA3: Power Management Techniques

Chair: *Xun Liu, North Carolina State University*
Co-chair: *Hongjiang Song, Intel Corporation*

1:30P Invited Paper: **"eXtreme Energy Conservation for Mobile Communications"**
TA3.1 *Christopher K. Y. Chun, Freescale Semiconductor*

1:55P **Compiler Support for Voltage Islands**
TA3.2 *Guangyu Chen, Mahmut Kandemir, Mustafa Karakoy*, Pennsylvania State University, *Department of Computing Imperial College London*

2:20P **Crosstalk-Aware Energy Efficient Encoding for Instruction Bus through Code Compression**
TA3.3 *Balaji Vaidyanathan, Yuan Xie, Pennsylvania State University*

SESSION TB3: Design Tools For SoC

Chair: *Kaijian Shi, Synopsys, Inc*
Co-chair: *Gi-Joon Nam, IBM Corporation*

1:30P Invited Paper: **"Platform-Based Behavior-Level and System-Level Synthesis"**
TB3.1 *Jason Cong, Yiping Fan, Guoling Han, Wei Jiang, Zhiru Zhang, UCLA*

1:55P **On Achieving Low-Power SoC Clock Tree Synthesis by Transition Time Planning via Buffer Library Study**
TB3.2 *Huang-Liang Chen and Hung-Ming Chen, National Chiao Tung University*

2:20P **Consideration of Transition-Time Variability in Statistical Timing Analysis**
TB3.3 *Takeshi Kouno and Hidetoshi Onodera, Kyoto University*

2:45P **Performance Constraints Aware Voltage Islands Generation in SoC Floorplan Design**
TB3.4 *Min-Ching Lu, Meng-Chen Wu*, Hung-Ming Chen*, and Hui-Ru Jiang*, SpringSoft Inc. *National Chiao Tung University*

3:10-3:30P COFFEE BREAK

3:30-5:30P **PANEL DISCUSSION:**
ORGANIZER: *Mike Boudreaux and John Chickanosky, IBM Corporation*

Abstract:

Moderator: *Mike Boudreaux*, *IBM Corporation*
Panelists: *Dr. Ronny Vasishta*, *CEO of eASIC*
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TUESDAY, SEPTEMBER 26

CONCURRENT SESSIONS
6:00 p.m. – 9:10 p.m.

6:00-8:00P **SPECIAL WORKSHOPS AND CONFERENCE RECEPTION**
Tutorial presentations

SOC 2010: Ubiquitous FPGAs
By: John B. Gallagher, Sr. Director, Outbound Marketing, Synplicity, Inc.

8:10PM – 9:10PM **TPC and OC Members Only Meeting**

WEDNESDAY, SEPTEMBER 27

CONCURRENT SESSIONS
8:30 a.m. – 10:10 a.m.

SESSION WA1: High Performance Digital Systems

Chair: *Koushik K. Das, IBM Corporation*

Co-chair: *Sundareswaran Savithri, Freescale*

8:30A **SOC Design Challenges in a Multi-threaded 65nm Dual Core Xeon® MP Processor**
WA1.1 *Raj Varada, Simon Tam, John Benoit, Kris Chou, Intel Corporation*

8:55A **Integration of Configurable Processors in a Multiprocessor Platform**
WA1.2 *Simon Provost, Bruno Lavigueur*, Guy Bois, Gabriela Nicolescu, École Polythechnique de Montréal, *STMicroelectronics*

9:20A **Crosstalk-aware Energy Reduction in NoC Communication Fabrics**
WA1.3 *Partha Pratim Pande, Haibo Zhu, Amlan Ganguly, Cristian Grecu*, Washington State University, *University of British Columbia*

9:45A **Interrupt Communication on the SegBus Platform**
WA1.4 *Appaya Devaraj Swaminathan and Tiberiu Seceleanu, University of Turku and TUCS*

SESSION WB1: Design for Testability, Manufacturability and Validation

Chair: *Fabrizio Lombardi, Northeastern University*

Co-chair: *Thomas Büchner, IBM*

8:30A **Fuse Area Reduction Based on Quantitative Yield Analysis and Effective Chip Cost**
WB1.1 *Akhil Garg, Prashant Dubey, ST Microelectronics*

8:55A **MTNet: Design and Optimization of A Wireless SoC Test Framework**
WB1.2 *Dan Zhao, Yi Wang, University of Louisiana at Lafayette*

9:20A **Modeling the Impact of Process Variation on Critical Charge Distribution**
WB1.3 *Qian Ding, Rong Luo, Hui Wang, Yuan Xie*, Huazhong Yang, Tsinghua University, China,* Pennsylvania State University*

9:45A **A Trace Based Framework for Validation of SoC Designs with GALS Systems**
WB1.4 *Syed Suhaib, Deepak Mathaikutty, and Sandeep Shukla, Virginia Tech*

10:10-10:30A COFFEE BREAK

WEDNESDAY, SEPTEMBER 27

CONCURRENT SESSIONS
10:30 a.m. – 11:45 a.m.

SESSION WA2: High Performance Digital Circuits

Chair: *Sanu Mathew, Intel Corporation*
Co-chair: *Tughrul Arslan, University of Edinburgh, Scotland, UK*

10:30A **Low-Power Priority Encoder and Multiple Match Detection Circuit for Ternary Content Addressable Memory**
WA2.1 *Nitin Mohan, Wilson Fung, and Manoj Sachdev, University of Waterloo*

10:55A **A 24-mW 0.02-mm² 1.5-GHz DLL-Based Frequency Multiplier in 130-nm CMOS**
WA2.2 *Behzad Mesgarzadeh and Atila Alvandpour, Linkoping University*

11:20A **Robust Sense Amplifier Design under Random Dopant Fluctuations in Nano-Scale CMOS Technologies**
WA2.3 *Joyce Yeung and Hamid Mahmoodi, San Francisco State University*

SESSION WB2: Wireline and Wireless Communications

Chair: *Sakir Sezer, Queen's University Belfast*
Co-chair: *Ken Hsu, Rochester Institute of Technology*

10:30A **Architecture for Energy Efficient Sphere Decoding**
WB2.1 *Ravi Jenkal, Hao Hua, Ambarish Sule, W. Rhett Davis, North Carolina State University*

10:55A **A Scalable Packet Sorting Circuit for High-Speed WFQ Packet Scheduling**
WB2.2 *K. McLaughlin, S. Sezer, H. Blume*, X. Yang, F. Kupzog*, T. Noll*, ECIT QUB,, *RWTH Aachen University*

11:20A **A MIMO Receiver SoC for CDMA Applications**
WB2.3 *Tongtong Chen, Zhengtao Yu, Yuantao Peng, Yanbin Zhang, Huaiyu Dai, Xun Liu, North Carolina State University*

11:45-1:30P LUNCH (on your own)

WEDNESDAY, SEPTEMBER 27

CONCURRENT SESSIONS
1:30 p.m. – 3:10 p.m.

SESSION WA3: Signal Integrity and On-Chip Interconnections

Chair: *Radu M. Secareanu, Freescale*
Co-chair: *Sundareswaran Savithri, Freescale*

1:30P Invited Paper: **"Effects of Interconnect Process Variations on Signal Integrity"**
WA3.1 *Ertugrul Demircan, Freescale Semiconductor Inc.*

1:55P **3-D Topologies for Networks-on-Chip**
WA3.2 *Vasilis F. Pavlidis and Eby G. Friedman, University of Rochester*

2:20P **A Low-swing Signaling Circuit Technique for 65nm On-chip Interconnects**
WA3.3 *Vishak Venkatraman, Mark Anders*, Himanshu Kaul*, Wayne Burleson, Ram Krishnamurthy*, University of Massachusetts Amherst, *Intel Corporation*

2:45P **Substrate and Ground Noise Interactions in Mixed-Signal Circuits**
WA3.4 *Emre Salman, Eby G. Friedman, Radu M. Secareanu*, University of Rochester, *Freescale Semiconductor MMSTL*

SESSION WB3: Embedded Memories

Chair: *Azeez Bhavnagarwala, IBM Corporation*
Co-chair: *Martin Margala, University of Rochester*

1:30P Invited Paper: **"Cache Organizations for Embedded Processors: CAM-vs-SRAM"**
WB3.1 *Baker Mohammad, Paul Bassett, Jacob Abraham*, and Adnan Aziz*, Qualcomm Inc., *University of Texas at Austin*

1:55P Invited Paper: "**Memories: Exploiting Them and Developing Them"**
WB3.2 *William Robert Reohr, IBM Corporation*

2:20P **Novel Ternary Storage Cells and Techniques for Leakage Reduction in Ternary CAM**
WB3.3 *Nitin Mohan and Manoj Sachdev, University of Waterloo*

2:45P **A Detailed Vth-Variation Analysis for Sub-100-nm Embedded SRAM Design**
WB3.4 *Masanao Yamaoka and Hidetoshi Onodera, Kyoto University*

3:10P **CONFERENCE ENDS**